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ROUTING OF VLSI CIRCUITS USING ANT COLONY OPTIMISATION**A.R.RAMAKRISHNAN****ASSOCIATE PROFESSOR****DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING****PSG COLLEGE OF TECHNOLOGY****COIMBATORE****V. RAJKUMAR****P.G. STUDENT****DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING****PSG COLLEGE OF TECHNOLOGY****COIMBATORE****ABSTRACT**

This paper discusses about VLSI routing that involves locating a set of paths to route wires, which connects all the terminals of the cells. Routing problem consists of connecting the terminals of the cells already placed on the chip, according to the given set of design specifications. The specifications involve the net-list, which indicates terminals to be interconnected. Efficient routing leads to reduction of total wire-length and hence active power consumption by minimizing the load capacitance of the chip. In this paper, Ant Colony Optimization [ACO] technique has been applied for routing process. Three benchmarks namely IBM, MCNC, ISCAS89 have been considered for testing the proposed algorithm. In this proposed methodology, a good reduction of wire-length is obtained for minimum number of pins with increased time over-head.

KEYWORDS

Routingproblem, netlist, powerconsumption, Ant colony, wire-length, Benchmark.

INTRODUCTION

The number of transistors on a VLSI chip, or IC chips to be interconnected is generally very large. The task of routing is to define path on the layout surface, on which conductors that carry electrical signals are run. These conductors (also called wiring segments) interconnect all the pins that are electrically equivalent. With rapid advancement in VLSI technology the number of transistors that can be placed on the single chip increased to about two billion. Such complex chips require power efficient design and advanced manufacturing techniques. One of the ways to minimize power consumption of the chip is to minimize the total wire length used for routing.

Routing in VLSI chips has been studied extensively and various routing methods have been proposed. Joobani [1], suggested an intelligence approach of routing wires based on the knowledge gained from the routers. These knowledge based routers avoid flaw with the help of guideline provided by the expert system, but consumes more time. Lienig [2], used genetic algorithm to minimize net-length, number of vias and crosstalk occurring due to the length of the parallel wires. Parallel approach of genetic algorithm showed better performance for channel and switch-box routing.

Yu Hu [3], suggested ACO-Steiner algorithm, where routing is performed by construction of Steiner points along with terminals and better minimization of wire-length is achieved compared to that of Lyet's [4] non-rectilinear Steiner tree algorithm. Kastner [5] uses predictable routing, commonly called Labyrinth Router, to perform global routing using pre-defined patterns in-order to estimate congested areas for routing nets. Here for the given number of nets, pattern routing is done for particular percentage of nets, followed by Maize routing for the remaining nets to provide accurate routing of all nets and wire length estimation, at the expense of longer running time. FastRoute [6], provides global routing solutions by reducing the congested areas for routing nets faster than Labyrinth router and less accurate wire-length estimations. FastRoute2.0 [7], is an improvement made for FastRoute resulting in faster run time compared to that of Labyrinth and good wire-length reduction compared to that of FastRoute at the expense of runtime. NTHU Router [8], outperforms Fastroute2.0 with improved wire-length reduction but consumes more runtime for routing nets.

The authors in this paper propose ACO based algorithm to find solutions that minimize wire length, and therefore power consumption.

ROUTING PROBLEM AND ACO**ROUTING PROBLEM**

The routing problem is defined as locating a set of paths to route wires that connect all the nets in the netlist. A net is a set of cells (also called terminal nodes) that need to be connected to each other in predefined manner. One of the important constraints that affects the efficiency and the usability of the chip is the power consumed by the chip. The power consumed by the chip is a function of capacitance determined by the equation $P = aCV^2f$, where a is an activity factor, V is voltage, f is frequency and C is capacitance due to wire-length. The main capacitance component is routed wires and hence the goal of this paper is to minimize the number of wires which in turn effectively reduces power consumption of the chip.

ANT COLONY OPTIMIZATION

Ant colony algorithms are developed from natural behaviour of real ants, particularly suited for the solution of optimization and control problems. ACO algorithms are inspired by foraging behaviour of ants and the indirect communication between them. Ants secrete a chemical substance called pheromone, that coordinates the ants while walking from food source to nest and vice-versa [9]. The trail marked by strong pheromone concentration tends the ants to choose the shortest path probabilistically between the nest and food source. Based on this context, ACO algorithms are derived with artificial ants and their indirect communications made by artificial pheromone. These pheromone trails make the ants to find all the possible shortest path between two points probabilistically with optimized solutions. For each execution of algorithm, the pheromones are modified [10, 11, 12] and the goodness of the path is based on the deposition of strong pheromone. The following gives an overview of the basic ACO algorithm [9].

ALGORITHM 1: ACO (Ant Colony Optimization)

1. Import the coordinates from benchmark circuit
2. Calculate the distance between each points
3. Initialize pheromone
4. {while (condition is not met)
5. Place ants at random position
6. {Initialize ant's memory
7. Start the route
8. {Using the pheromone and heuristics values calculate the probability to visit the nodes

9. } update the visited node in ant's memory
10. } Find the best route
11. Update pheromone
12. }}

IMPLEMENTATION OF ACO ALGORITHM FOR VLSI ROUTING

In this section, ACO algorithm underlying assumptions and methods followed for the implementation are discussed. This work uses the following Benchmark sets to perform routing.

BENCHMARK SETS

There exists several different formats to specify input format to the router[13].These benchmark provides the placement of the node that should be routed with shortest path .This work uses following set of benchmark suites namely,

- a) R1,R2 benchmarks of IBM from R.S.Tsay [14] [15].
- b) Prim 1, Prim 2 benchmarks of MCNC from Jackson et al [16][17].
- c) S1423 ,S5378 ,S15850 benchmarks of ISCAS89 benchmarks from J.G. Xi et al[18][19][20].

These benchmark circuits consists of net-list that provide information of nets to be interconnected. The process of routing nets are as follows.

ROUTING NETS

From the given net-list, the ants are distributed randomly on the available nodes to be routed. The distance between the nodes are calculated initially. The number of ants on the node and other ACO parameters like α (pheromone parameter), β (desirability parameter), and ρ (Pheromone update-evaporation constant) are varied according to the best solution. The ant's memory are initialized and current node on which the ant is placed is updated in ant's memory. The probability of ant to choose shortest path depends upon the pheromone amount and desirability of the path. The shortest path made by the ant results in reduced wire-length.

DESIRABILITY

The desirability of the ant to visit the node depends upon the distance between the two nodes and hence defined as the minimum distance between current node i , where ant is located to the node yet to be visited j and all other remaining ants belonging to the same net

$$\alpha \eta_{i,dir} = \frac{1}{\text{Min} [\alpha D_{i,j}, \alpha D_{i,k}, \alpha D_{i,l}, \alpha D_{i,m}]} \quad (1)$$

where α' is the terminal node from where the current ant started, i is the current node of the ant that started at α' , dir is the next node decided by this function, which is not yet already visited, $\alpha D_{i,j}$ is the total distance between ant's next node j and all other ants when the previous given node is i and can be defined as:

$$\alpha' D_{i,j} = [\sum_{a=i}^n M_{i,\alpha} + M_{x,i}] \text{ For } a \neq \alpha' \quad (2)$$

here $M_{i,\alpha}$ is the Manhattan distance between point ' i ' and ' α ' and α is the current position for other ants of the net.

PROBABILITY

Thus the probability of choosing an arc (i, j) could be defined as following

$$P_{i,j} = \frac{(\tau_{i,j}^\alpha) (\eta_{i,j}^\beta)}{\sum (\tau_{i,j}^\alpha) (\eta_{i,j}^\beta)} \quad (3)$$

Where $P_{i,j}$ is the probability that an ant at node i will move to node j , $\tau_{i,j}$ is the amount of pheromone on path i, j , $\eta_{i,j}$ is the desirability of any path i, j , α parameter to control the influence of $\tau_{i,j}$, β is the parameter to control the influence of $\eta_{i,j}$. After calculating desirability and probability, ants starts traversing the path and connects the nets as described by the net-list, followed by the pheromone update.

PHEROMONE UPDATE

Pheromone update is done in order to choose the best shortest path across different iteration. Here the deposited pheromones are first evaporated by a constant factor ρ and given by the equation,

$$\tau_{i,j} = (1 - \rho) \tau_{i,j} \quad (4)$$

Next pheromone update is done only for the best ant after each iteration and hence it can be denoted as the function of tour length traversed by best ant given by the equation

$$\Delta \tau_{i,j}^{bs} = 1/c^{bs} \quad (5)$$

Where $\Delta \tau_{i,j}^{bs}$ is the amount of pheromone deposited on the path taken by the best ant of the iteration and c^{bs} is the tour length traversed by the best ant.

Therefore, the pheromone update could be represented as:

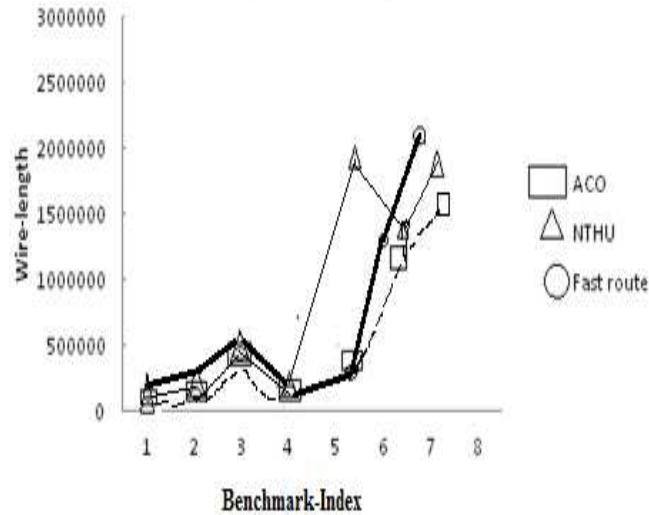
$$\tau_{i,j} = (1 - \rho) \tau_{i,j} + \rho \Delta \tau_{i,j}^{bs} \quad (6)$$

EXPERIMENTS AND ANALYSIS

The ACO algorithm for routing has been coded in MATLAB and the experiments are executed on a 2.40 GHz Intel core i3 processor. The three main parameters that affect any ACO algorithm is the choice of alpha (α), beta (β) and rho (ρ). A good parameter setting maintains a balance between the focus of the search and exploration of new paths during the search. Whereas a bad parameter setting will make the search either too narrow and focused leading to stagnation behaviour or could cause excessive exploration of search paths leading to a never converging search process. Thus to find a suitable value of parameters that maintains the balance between the focus and explorative nature of the search the difference between tour lengths was measured for various nets with many different sets of parameter values as indicated in table 1 . The set of parameter values that provided a good improvement in performance with the iterations of the algorithm was chosen.

The number of ants used in an ACO algorithm depends on the number of nodes of the search graph and has a direct influence on the computation time of the algorithm. More ants per node are able to perform a more exhaustive search compared to fewer ants, but also require more time for computation. Thus, there exists a trade-off between the computation time and performance of the ACO-route algorithm. This trade-off exists only until the number of ants used in the algorithm is below saturation value beyond which performance does not improve. If the average number of ants per node is increased beyond this saturation value, the increased number of ants tends to reinforce the locally optimum solution. Beyond this value, the only affect of the increase in number of ants is to increase the computational time of the algorithm .Same effect is experienced in performing the iterations as shown in table 2. Three types of benchmark suites were tested and summarised results are shown in table 3. From the table we can infer that From the result we can infer that if number of pins are increased , correspondingly wire-length also increases with inherent time period. The reason is due to routing done on single layer. In contrary , if multi-routing layer are introduced , there can be a rapid decrease in wire-length accompanied by the reduction of power consumption. Figure1 illustrates the wire-length of ACO route, NTHU route and Fast route. The wire-length of NTHU route is of maximum unit compared to that of other two routers.ACO has a low wire-length at the expense of time period, compared to that of Fast route and still can be minimized by using multi-routing layers.

FIGURE 1: COMPARISON OF WIRE-LENGTHS WITH BENCHMARKS



Benchmark Index[1-S1423; 2-S5378; 3-S15850; 4-Prim1; 5-prim2; 6-R1; 7-R2]

TABLE 1: DIFFERENT SETS OF PARAMETER VALUES

| Benchmark S1423 status | Alpha | Beta | Rho | Wire-length(unit) |
|------------------------|-------|------|------|-------------------|
| Normal | 1 | 5 | 0.5 | 72792 |
| Above | 2 | 10 | 1 | 74285 |
| Below | 0.5 | 2.25 | 0.25 | 85998 |

TABLE 2: NUMBER OF ANTS PER NODE AND NUMBER OF ITERATIONS PERFORMED

| Benchmark S1423 Status | No of Iteration | No of ants | Wire-length(units) |
|------------------------|-----------------|------------|--------------------|
| Normal | 100 | 74 | 72792 |
| Above | 200 | 128 | 72479 |
| Below | 50 | 37 | 74601 |

TABLE 3: COMPARISON OF ACO –ROUTE WIRE-LENGTH WITH TIME PERIOD

| Provider | Benchmark Name | Fast Route | | NTHU Route | | ACO Route | |
|----------|------------------|-------------------|------------|--------------------|------------|--------------------|------------|
| | | WireLength (Unit) | Time(Secs) | Wire-Length (Unit) | Time(Secs) | Wire-Length (Unit) | Time(Secs) |
| ISCAS'89 | S1423 (74 pins) | 107277 | 0.72 | 91605 | 4.17 | 72792 | 119 |
| | S5378 (179 pins) | 176517 | 0.93 | 146874 | 7.44 | 138379 | 207 |
| | S15850 (579ns) | 359990 | 1.6 | 315474 | 5.98 | 363841 | 321 |
| MCNC | Prim 1 (269ns) | 131463 | 1.52 | 115500 | 13.17 | 109793 | 412 |
| | Prim 2 (603ns) | 268681 | 1.92 | 2446976 | 15.59 | 303613 | 626 |
| IBM | R1 (267ns) | 1320665 | 1.46 | 1230884 | 12.22 | 1084887 | 408 |
| | R2 (598 pins) | 2169791 | 1.88 | 1918561 | 13.61 | 2149532 | 551 |

CONCLUSION AND FUTURE SCOPE

The goal of this work is to minimise the length of wires used in routing. Routing of VLSI chips is an NP complete optimization problem. An algorithm using an Ant Colony Optimization technique was developed for solving the constraint of optimizing wire-length and thereby the load capacitance. Adjusting and fixing the controlling parameters like alpha, beta, and rho yields good reduction of wire-length. Moreover saturate level of number of iterations and number of ants per node provides comparable reduction of wire-length. For minimum number of pins better reduction of wire-length was achieved. However there is significant room to enhance the algorithm and widen the domain to which it applies. Implementation of Algorithm in multi-layered path which has advantage of reduction of wire-length, naturally decreases capacitance and in-turn reduce active power component . Hence more number of pins can be accommodated and algorithm can be implemented with different architecture.

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