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AREA EFFICIENT APPROACH FOR 64-BIT MULTIPLICATION USING CONFIGURABLE DEVICES

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ABSTRACT

Multiplication and division are the two elementary operations essential for the core computing process or for the arithmetic operation. These two operations are also the most critical functions carried out by the processors as the multiplication requires more number of steps for the computation, limiting the overall performance of the system, and the division has the highest latency among all arithmetic operations. Thus, high performance multiplication and division algorithms/ architectures, if available, will considerably improve the speeds of processing system. Consequently, the need for faster processing of arithmetic operations, is continuously driving major improvements in processor technologies. This work attempts to design such hardware architecture for double precision floating-point multiplication that is easily implementable with high efficiency. The multiplier unit is based on ancient Vedic mathematics technique. The proposed design is described using VHDL. The code description is simulated on reconfigurable device using Modelsim SE 5.7f and synthesized using ISE Xilinx 10.1i for the FPGA device Virtex -XC4V5X25-12FF668.

KEYWORDS

Multiplier, Double Precision, Configurable, Floating point, FPGA.

1. INTRODUCTION

With the rapid development and wide application of computer technology, high performance applications have become extremely popular in modern computer systems, requiring enhanced computation capabilities at low cost and power consumption. Also, in contemporary signal processing and communication applications, a high throughput rate and numerical accuracy is often demanded. One of the important requirements in such applications is to perform a large number of mathematical calculations in a very less time. That is, faster computational methods are vastly claimed for advancement in technology.

Multiplication and division are the two elementary operations essential for the core computing process or for the arithmetic operation. These two operations are also the most critical functions carried out by the processors, as the multiplication requires more number of steps for the computation, limiting the overall performance of the system, and the division has the highest latency among all arithmetic operations. Thus, high performance multiplication and division algorithms/ architectures, if available, will considerably improve the speeds of processing system. Consequently, the need for faster processing of arithmetic operations, is continuously driving major improvements in processor technologies, as well as the search for new arithmetic algorithms. This work attempts to design such hardware architecture for double precision floating-point multiplication [1,2] that is easily implementable with high efficiency. The multiplier unit is based on ancient Vedic mathematics [3] technique. The proposed design is described using VHDL. The code description is simulated on reconfigurable device using Modelsim SE 5.7f and synthesized using ISE Xilinx 10.1i for the FPGA device Virtex -XC4V5X25-12FF668.

This paper is organized in the following way: Section II highlights the related work. In Section III a brief review of IEEE 754 standard for binary floating-point arithmetic is given. Then in section IV, the synthesis results is demonstrated. Finally, in section V the paper is concluded with the applications of the operators and prospects for future improvements in these implementations.

2. BRIEF SUMMARY OF PREVIOUS WORK

Earlier work was presented [4] for 24*24 multiplier in which they used digit-serial arithmetic which is not so fast method. Also, proper rounding techniques were not implemented. However, they presented a pipelined structure in order to produce a result every clock cycle. A work for floating-point division is reported [5] for embedded VLSI integer processors with no hardware unit. They focused on high-radix digit-recurrence algorithms. In these implementations, 32 bit operators are designed. However, by using a small floating point format (16 bits or 18 bits wide), smaller and faster implementations can be built but with less accuracy.

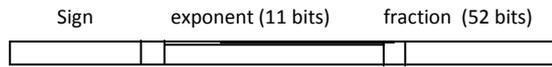
There are number of problems associated with tree and array multipliers [6]. Tree multipliers have shortest logic delay but irregular layouts with complicated interconnects. Irregular layouts introduce significant interconnect delay and make noise a problem and the delay of the interconnection is not suitable for VLSI implementation. Similarly array multipliers have larger delay and significant amount of power is consumed.

Transistor level implementation of Vedic Mathematics based 32-bit multiplier for high speed low power processor was suggested by [7]. Simple Boolean logic is combined with 'Vedic' formulas, which reduces the partial products and sums generated in one step, reduces the carry propagation from LSB to MSB. The implementation methodology ensure substantial reduction of propagation delay in comparison with Wallace Tree, modified Booth Algorithm, Baugh Wooley and Row Bypassing and Parallel Architecture based implementation which are most commonly used architectures. The functionality of these circuits was checked and performance parameters like propagation delay and dynamic power consumption were calculated by spice spectre using standard 90nm CMOS technology.

3. DOUBLE PRECISION FLOATING POINT FORMAT

The IEEE Standard for Binary Floating-Point Arithmetic (IEEE 754) is the most widely-used standard for floating-point computation, and is followed by many CPU and FPU implementations. The standard defines formats for representing floating-point numbers (including negative zero and denormal numbers) and special values (infinities and NaNs) together with a set of floating-point operations that operate on these values. It also specifies four rounding modes and five exceptions (including when the exceptions occur, and what happens when they do occur). Four formats for representing floating-point values are: single-precision (32-bit), double-precision (64-bit), single-extended precision (≥ 43 -bit, not commonly used) and double-extended precision (≥ 79 -bit, usually implemented with 80 bits). The basic format for single precision is further divided into sign, exponent, and mantissa part as shown in Fig 3.1.

FIG 3.1: FORMAT FOR DOUBLE-PRECISION MULTIPLIER



3.1 Normalized Numbers [8]

In most cases, the floating-point real numbers are represented in normalized form. A normalized real number consists of a normalized significand that represents a real number between 1 and 2 and an exponent that specifies the number's binary point. The requirement that the leftmost digit of the significand be nonzero is called normalization.

3.2 Real Numbers and non number Encodings

A variety of real numbers and special values can be encoded in floating-point format. These numbers and values are generally divided into the following classes:

1. Signed Zeros

Zero can be represented as a +0 or a -0 depending on the sign bit. Both encodings are equal in value. The sign of a zero result depends on the operation being performed and the rounding mode being used.

2. Normalized and Denormalized Finite Numbers

Non-zero, finite numbers are divided into two classes: normalized and denormalized. The normalized finite numbers comprise all the non-zero finite values that can be encoded in a normalized real number format between zero and infinity (∞). The denormalized number is computed through a technique called gradual underflow.

3. Signed Infinities

The two infinities, +∞ and -∞, represent the maximum positive and negative real numbers, respectively, that can be represented in the floating-point format. Infinity is always represented by a zero significand (fraction and integer bit) and the maximum biased exponent allowed in the specified format

4. Not a Number (NaN)

There are two classes of NaN: quiet NaNs (QNaNs) and signaling NaNs (SNaNs). A QNaN is a NaN with the most significant fraction bit set; a SNaN is a NaN with the most significant fraction bit clear.

5. Indefinite

For each FPU data type, one unique encoding is reserved for representing the special value indefinite.

3.3 Conversion and Rounding

When a number is represented in some other format (such as a string of digits), then it will require a conversion to be used in floating-point format. When the result is obtained from an operation, it may not be possible to represent exactly in the IEEE 754 standard. Therefore, rounding is needed before the result is stored in the memory or registers, and/or sent to the output. In round to nearest even the value is rounded up or down to the nearest infinitely precise result. In round up and down the number will be rounded up towards +∞ and -∞ respectively. Round towards zero modes is not used in general.

3.4 Exceptions

There are four types of exceptions that should be signaled through a one bit status flag when encountered. Some arithmetic operations are invalid, such as a division by zero or square root of a negative number. The result of an invalid operation shall be a NaN.

Inexact exception should be signaled whenever the result of an arithmetic operation is not exact due to the restricted exponent and/or precision range. Two events cause the underflow exception to be signaled, tininess and loss of accuracy. The overflow exception is signaled whenever the result exceeds the maximum value that can be represented due to the restricted exponent range. It is not signaled when one of the operands is infinity, because infinity arithmetic is always exact.

3.5 Multiplication Algorithm

A binary floating-point number is represented by a sign bit, the significand and the exponent. Given two numbers Operand A and Operand B, the flowchart in figure 2 can be used to compute their product, given that e_A, e_B and frac_A, frac_B are the exponents and significands of the numbers, respectively. A detailed description of the algorithm follows:

1. The hidden bit (24th bit) is made explicit. If e_A or e_B = 0, it is made '0', otherwise a '1'.
2. The result of the multiplication is given by the formula:

$$\text{Sign} = \text{sign}_A \text{ xor } \text{sign}_B, e = e_A + e_B,$$

$$\text{Frac} = \text{frac}_A \times \text{frac}_B$$

The addition of the exponents is a trivial operation as long as we keep in mind that they are biased. This means that in order to get the right result, we have to subtract 127 (bias) from their sum. The sign of the result is just the XOR of the two sign bits. The multiplication of the significands is just an unsigned, integer multiplication.

3. There must be a leading '1' in the significand of any floating-point number (unless it is not denormalized). To make the MSB '1' in the result, the bits are shifted left, and with each shift, the exponent is incremented by 1. This way normalization is done.

3.6 Vedic Multiplier

The multiplier A[n] is of size 'n' words and the multiplicand B[m] is of size 'm' words, where A and B are given by equation 1 and 2.

$$A[n] = \sum_{i=0}^{n-1} a_i * X^i \tag{1}$$

$$B[m] = \sum_{i=0}^{m-1} b_i * X^i \tag{2}$$

Product of A and B is given by equation 3.

$$P [n + m] = A [n] * B [m] \tag{3}$$

$$\sum_{i=1}^n CP[0,0,i] * X^{i-1} +$$

$$\sum_{j=1}^{m-n} CP[0,j,n] * X^{n+j-1} +$$

$$\sum_{k=1}^{n-1} CP[k,k+m-n,n-k] * X^{m+k+1}$$

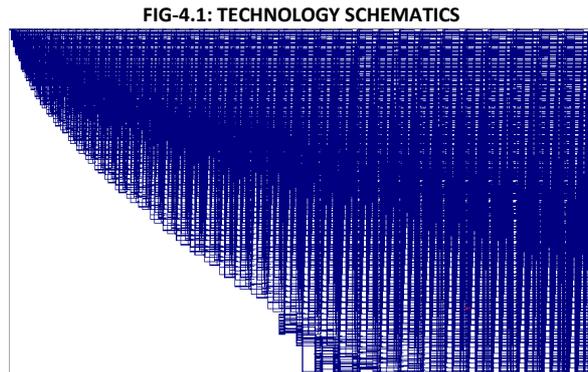
Where

$$CP[n,m,q] = \sum_{i=n}^{n+q-1} a_i * b_j \tag{4}$$

Equation 4 gives the cross-product of two numbers. where j = (m + n + q - i - 1)

4. RESULTS

The code is written in HDL, synthesized and simulated using Virtex 4 (Device : xc4vsx35-10-ff668) and speed grade of -12. Technology schematics is shown in Fig. 4.1.



Synthesis results shows 12447 slices are used out of 15360, 22789 numbers of 4 input LUTs are used out of 30720 and number of bonded IOBs are 195 out of 448. This is shown in Fig.4.2.

FIG-4.2: SYNTHESIS RESULTS

Device Utilization Summary (estimated values)				
Logic Utilization	Used	Available	Utilization	
Number of Slices	12447	15360		81%
Number of Slice Flip Flops	144	30720		0%
Number of 4 input LUTs	22789	30720		74%
Number of bonded IOBs	195	448		43%
Number of GCLKs	1	32		3%

Macro Statistics details are given below:

- # Adders/Subtractors : 252
- 9-bit adder : 103
- 12-bit adder : 2
- 12-bit subtractor : 1
- 16-bit adder : 1
- 17-bit adder : 4
- 18-bit adder : 14

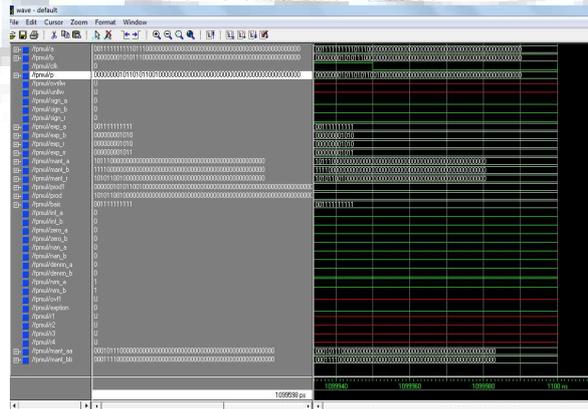
5. CONCLUSION

In this paper, it is shown that double precision floating point multiplier is synthesized and simulated using Configurable devices. The presented implementations give

- 19-bit adder : 29
- 9-bit adder : 49
- # Registers : 18
- 1-bit register : 15
- 12-bit register : 1
- 53-bit register : 1
- 64-bit register : 1
- # Comparators : 8
- 12-bit comparator greater : 2
- 12-bit comparator less : 2
- 53-bit comparator equal : 2
- 53-bit comparator greater : 2
- # Multiplexers : 1
- 109-bit 4-to-1 multiplexer : 1
- # Xors : 5538
- 1-bit xor2 : 5538
- 8 bit adder : 49

Timing report summary indicates total time taken for process is 203.817 ns out of which 79,879 ns are used for logic and 18.755ns are utilized for routing. Simulation Results are shown in Fig. 4.3.

FIG-4.3: SIMULATION RESULTS



Since area and speed of the design is always a main concern, finding possible ways of customizing our design in terms of timing delay and slices has been tried and this can also be a future enhancement of the present work. In the end, it can be perceived that such a design can enable substantial savings of resources in the FPGA when used for signal processing applications.

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