INTERNATIONAL JOURNAL OF RESEARCH IN COMPUTER APPLICATION & MANAGEMENT

IJRCM

A Monthly Double-Blind Peer Reviewed (Refereed/Juried) Open Access International e-Journal - Included in the International Serial Directories

Indexed & Listed at:

Ulrich's Periodicals Directory ©, ProQuest, U.S.A., EBSCO Publishing, U.S.A., Cabell's Directories of Publishing Opportunities, U.S.A.,

Open J-Gage, India [link of the same is duly available at Inflibnet of University Grants Commission (U.G.C.)],

Index Copernicus Publishers Panel, Polandwith IC Value of 5.09 &number of libraries all around the world.

Circulated all over the world & Google has verified that scholars of more than 2477 Cities in 159 countries/territories are visiting our journal on regular basis.

Ground Floor, Building No. 1041-C-1, Devi Bhawan Bazar, JAGADHRI – 135 003, Yamunanagar, Haryana, INDIA

http://ijrcm.org.in/

CONTENTS

CALL FOR MANUSCRIPTS

Weinvite unpublished novel, original, empirical and high quality research work pertaining to recent developments & practices in the area of Computer, Business, Finance, Marketing, Human Resource Management, General Management, Banking, Education, Insurance, Corporate Governance and emerging paradigms in allied subjects like Accounting Education; Accounting Information Systems; Accounting Theory & Practice; Auditing; Behavioral Accounting; Behavioral Economics; Corporate Finance; Cost Accounting; Econometrics; Economic Development; Economic History; Financial Institutions & Markets; Financial Services; Fiscal Policy; Government & Non Profit Accounting; Industrial Organization; International Economics & Trade; International Finance; Macro Economics; Micro Economics; Monetary Policy; Portfolio & Security Analysis; Public Policy Economics; Real Estate; Regional Economics; Tax Accounting; Advertising & Promotion Management; Business Education; Management Information Systems (MIS); Business Law, Public Responsibility & Ethics; Communication; Direct Marketing; E-Commerce; Global Business; Health Care Administration; Labor Relations & Human Resource Management; Marketing Research; Marketing Theory & Applications; Non-Profit Organizations; Office Administration/Management; Operations Research/Statistics; Organizational Behavior & Theory; Organizational Development; Production/Operations; Public Administration; Purchasing/Materials Management; Retailing; Sales/Selling; Services; Small Business Entrepreneurship; Strategic Management Policy; Technology/Innovation; Tourism, Hospitality & Leisure; Transportation/Physical Distribution; Algorithms; Artificial Intelligence; Compilers & Translation; Computer Aided Design (CAD); Computer Aided Manufacturing; Computer Graphics; Computer Organization & Architecture; Database Structures & Systems; Digital Logic; Discrete Structures; Internet; Management Information Systems; Modeling & Simulation; Multimedia; Neural Systems/Neural Networks; Numerical Analysis/Scientific Computing; Object Oriented Programming; Operating Systems; Programming Languages; Robotics; Symbolic & Formal Logic and Web Design. The above mentioned tracks are only indicative, and not exhaustive.

Anybody can submit the soft copy of his/her manuscript **anytime** in M.S. Word format after preparing the same as per our submission guidelines duly available on our website under the heading guidelines for submission, at the email address: infoijrcm@gmail.com.

GUIDELINES FOR SUBMISSION OF MANUSCRIPT

1. **COVERING LETTER FOR SUBMISSION:**

DATED: _____

THE EDITOR
IJRCM

Subject: **SUBMISSION OF MANUSCRIPT IN THE AREA OF .**

(e.g. Finance/Marketing/HRM/General Management/Economics/Psychology/Law/Computer/IT/Engineering/Mathematics/other, please specify)

DEAR SIR/MADAM

Please find my submission of manuscript entitled '_____' for possible publication in your journals.

I hereby affirm that the contents of this manuscript are original. Furthermore, it has neither been published elsewhere in any language fully or partly, nor is it under review for publication elsewhere.

I affirm that all the author (s) have seen and agreed to the submitted version of the manuscript and their inclusion of name (s) as co-author (s).

Also, if my/our manuscript is accepted, I/We agree to comply with the formalities as given on the website of the journal & you are free to publish our contribution in any of your journals.

NAME OF CORRESPONDING AUTHOR:
Designation:
Affiliation with full address, contact numbers & Pin Code:
Residential address with Pin Code:
Mobile Number (s):
Landline Number (s):
E-mail Address:
Alternate E-mail Address:

NOTES:

a) The whole manuscript is required to be in ***ONE MS WORD FILE*** only (pdf. version is liable to be rejected without any consideration), which will start from the covering letter, inside the manuscript.
b) The sender is required to mentionthe following in the **SUBJECT COLUMN** of the mail:
New Manuscript for Review in the area of (Finance/Marketing/HRM/General Management/Economics/Psychology/Law/Computer/IT/ Engineering/Mathematics/other, please specify)
c) There is no need to give any text in the body of mail, except the cases where the author wishes to give any specific message w.r.t. to the manuscript.
d) The total size of the file containing the manuscript is required to be below **500 KB**.
e) Abstract alone will not be considered for review, and the author is required to submit the complete manuscript in the first instance.
f) The journal gives acknowledgement w.r.t. the receipt of every email and in case of non-receipt of acknowledgment from the journal, w.r.t. the submission of manuscript, within two days of submission, the corresponding author is required to demand for the same by sending separate mail to the journal.

2. **MANUSCRIPT TITLE:** The title of the paper should be in a 12 point Calibri Font. It should be bold typed, centered and fully capitalised.

3. **AUTHOR NAME (S) & AFFILIATIONS:** The author (s) **full name**, **designation**, **affiliation** (s), **address**, **mobile/landline numbers**, and **email/alternate email address** should be in italic & 11-point Calibri Font. It must be centered underneath the title.

4. **ABSTRACT:** Abstract should be in fully italicized text, not exceeding 250 words. The abstract must be informative and explain the background, aims, methods, results & conclusion in a single para. Abbreviations must be mentioned in full.

5. **KEYWORDS:** Abstract must be followed by a list of keywords, subject to the maximum of five. These should be arranged in alphabetic order separated by commas and full stops at the end.

6. **MANUSCRIPT:** Manuscript must be in ***BRITISH ENGLISH*** prepared on a standard A4 size ***PORTRAIT SETTING PAPER***. It must be prepared on a single space and single column with 1" margin set for top, bottom, left and right. It should be typed in 8 point Calibri Font with page numbers at the bottom and centre of every page. It should be free from grammatical, spelling and punctuation errors and must be thoroughly edited.

7. **HEADINGS:** All the headings should be in a 10 point Calibri Font. These must be bold-faced, aligned left and fully capitalised. Leave a blank line before each heading.

8. **SUB-HEADINGS:** All the sub-headings should be in a 8 point Calibri Font. These must be bold-faced, aligned left and fully capitalised.

9. **MAIN TEXT:** The main text should follow the following sequence:

INTRODUCTION

REVIEW OF LITERATURE

NEED/IMPORTANCE OF THE STUDY

STATEMENT OF THE PROBLEM

OBJECTIVES

HYPOTHESES

RESEARCH METHODOLOGY

RESULTS & DISCUSSION

FINDINGS

RECOMMENDATIONS/SUGGESTIONS

CONCLUSIONS

SCOPE FOR FURTHER RESEARCH

ACKNOWLEDGMENTS

REFERENCES

APPENDIX/ANNEXURE

It should be in a 8 point Calibri Font, single spaced and justified. The manuscript should preferably not exceed ***5000 WORDS***.

10. **FIGURES &TABLES:** These should be simple, crystal clear, centered, separately numbered &self explained, and **titles must be above the table/figure**. **Sources of data should be mentioned below the table/figure**. It should be ensured that the tables/figures are referred to from the main text.

11. **EQUATIONS:**These should be consecutively numbered in parentheses, horizontally centered with equation number placed at the right.

12. **REFERENCES:** The list of all references should be alphabetically arranged. The author (s) should mention only the actually utilised references in the preparation of manuscript and they are supposed to follow **Harvard Style of Referencing**. The author (s) are supposed to follow the references as per the following:

- All works cited in the text (including sources for tables and figures) should be listed alphabetically.
- Use (**ed.**) for one editor, and (**ed.s)** for multiple editors.
- When listing two or more works by one author, use --- (20xx), such as after Kohl (1997), use --- (2001), etc, in chronologically ascending order.
- Indicate (opening and closing) page numbers for articles in journals and for chapters in books.
- The title of books and journals should be in italics. Double quotation marks are used for titles of journal articles, book chapters, dissertations, reports, working papers, unpublished material, etc.
- For titles in a language other than English, provide an English translation in parentheses.
- The location of endnotes within the text should be indicated by superscript numbers.

PLEASE USE THE FOLLOWING FOR STYLE AND PUNCTUATION IN REFERENCES:

BOOKS

- Bowersox, Donald J., Closs, David J., (1996), "Logistical Management." Tata McGraw, Hill, New Delhi.
- Hunker, H.L. and A.J. Wright (1963), "Factors of Industrial Location in Ohio" Ohio State University, Nigeria.

CONTRIBUTIONS TO BOOKS

- Sharma T., Kwatra, G. (2008) Effectiveness of Social Advertising: A Study of Selected Campaigns, Corporate Social Responsibility, Edited by David Crowther & Nicholas Capaldi, Ashgate Research Companion to Corporate Social Responsibility, Chapter 15, pp 287-303.

JOURNAL AND OTHER ARTICLES

- Schemenner, R.W., Huber, J.C. and Cook, R.L. (1987), "Geographic Differences and the Location of New Manufacturing Facilities," Journal of Urban Economics, Vol. 21, No. 1, pp. 83-104.

CONFERENCE PAPERS

- Garg, Sambhav (2011): "Business Ethics" Paper presented at the Annual International Conference for the All India Management Association, New Delhi, India, 19–22 June.

UNPUBLISHED DISSERTATIONS AND THESES

- Kumar S. (2011): "Customer Value: A Comparative Study of Rural and Urban Customers," Thesis, KurukshetraUniversity, Kurukshetra.

ONLINE RESOURCES

- Always indicate the date that the source was accessed, as online resources are frequently updated or removed.

WEBSITES

- Garg, Bhavet (2011): Towards a New Natural Gas Policy, Political Weekly, Viewed on January 01, 2012 http://epw.in/user/viewabstract.jsp

AREA EFFICIENT APPROACH FOR 64-BIT MULTIPLICATION USING CONFIGURABLE DEVICES

DINESH KUMAR
ASSOCIATE PROFESSOR
ECE DEPARTMENT
M. M. ENGINEERING COLLEGE
M. M. UNIVERSITY
MULLANA

G.C. LALL
PROFESSOR
ECE DEPARTMENT
HARYANA COLLEGE OF TECHNOLOGY & MANAGEMENT
KAITHAL

ABSTRACT

Multiplication and division are the two elementary operations essential for the core computing process or for the arithmetic operation. These two operations are also the most critical functions carried out by the processors as the multiplication requires more number of steps for the computation, limiting the overall performance of the system, and the division has the highest latency among all arithmetic operations. Thus, high performance multiplication and division algorithms/ architectures, if available, will considerably improve the speeds of processing system. Consequently, the need for faster processing of arithmetic operations, is continuously driving major improvements in processor technologies. This work attempts to design such hardware architecture for double precision floating-point multiplication that is easily implementable with high efficiency. The multiplier unit is based on ancient Vedic mathematics technique. The proposed design is described using VHDL. The code description is simulated on reconfigurable device using Modelsim SE 5.7f and synthesized using ISE Xilinx 10.1i for the FPGA device Virtex -XC4VSX25-12FF668.

KEYWORDS
Multiplier, Double Precision, Configurable, Floating point, FPGA.

1. INTRODUCTION

With the rapid development and wide application of computer technology, high performance applications have become extremely popular in modern computer systems, requiring enhanced computation capabilities at low cost and power consumption. Also, in contemporary signal processing and communication applications, a high throughput rate and numerical accuracy is often demanded. One of the important requirements in such applications is to perform a large number of mathematical calculations in a very less time. That is, faster computational methods are vastly claimed for advancement in technology.

Multiplication and division are the two elementary operations essential for the core computing process or for the arithmetic operation. These two operations are also the most critical functions carried out by the processors , as the multiplication requires more number of steps for the computation, limiting the overall performance of the system, and the division has the highest latency among all arithmetic operations. Thus, high performance multiplication and division algorithms/ architectures, if available, will considerably improve the speeds of processing system. Consequently, the need for faster processing of arithmetic operations, is continuously driving major improvements in processor technologies, as well as the search for new arithmetic algorithms.This work attempts to design such hardware architecture for double precision floating-point multiplication [1,2] that is easily implementable with high efficiency. The multiplier unit is based on ancient vedic mathematics [3] technique. The proposed design is described using VHDL. The code description is simulated on reconfigurable device using Modelsim SE 5.7f and synthesized using ISE Xilinx 10.1i for the FPGA device Virtex -XC4VSX25-12FF668.

This paper is organized in the following way: Section II highlights the related work. In Section III a brief review of IEEE 754 standard for binary floating-point arithmetic is given. Then in section IV, the synthesis results is demonstrated. Finally, in section V the paper is concluded with the applications of the operators and prospects for future improvements in these implementations.

2. BRIEF SUMMARY OF PREVIOUS WORK

Earlier work was presented [4] for 24*24 multiplier in which they used digit-serial arithmetic which is not so fast method. Also, proper rounding techniques were not implemented. However, they presented a pipelined structure in order to produce a result every clock cycle. A work for floating-point division is reported [5] for embedded VLSI integer processors with no hardware unit. They focused on high-radix digit-recurrence algorithms. In these implementations, 32 bit operators are designed. However, by using a small floating point format (16 bits or 18 bits wide), smaller and faster implementations can be built but with less accuracy.

There are number of problems associated with tree and array multipliers [6]. Tree multipliers have shortest logic delay but irregular layouts with complicated interconnects. Irregular layouts introduce significant interconnect delay and make noise a problem and the delay of the interconnection is not suitable for VLSI implementation. Similarly array multipliers have larger delay and significant amount of power is consumed.

Transistor level implementation of Vedic Mathematics based 32-bit multiplier for high speed low power processor was suggested by [7]. Simple Boolean logic is combined with 'Vedic' formulas, which reduces the partial products and sums generated in one step, reduces the carry propagation from LSB to MSB. The implementation methodology ensure substantial reduction of propagation delay in comparison with Wallace Tree , modified Booth Algorit, Baugh Wooley and Row Bypassing and Parallel Architecture based implementation which are most commonly used architectures. The functionality of these circuits was checked and performance parameters like propagation delay and dynamic power consumption were calculated by spice spectre using standard 90nm CMOS technology.

3. DOUBLE PRECISION FLOATING POINT FORMAT

The IEEE Standard for Binary Floating-Point Arithmetic (IEEE 754) is the most widely-used standard for floating-point computation, and is followed by many CPU and FPU implementations. The standard defines formats for representing floating-point numbers (including negative zero and denormal numbers) and special values (infinities and NaNs) together with a set of floating-point operations that operate on these values. It also specifies four rounding modes and five exceptions (including when the exceptions occur, and what happens when they do occur). Four formats for representing floating-point values are: single-precision (32-bit), double-precision (64-bit), single-extended precision (≥ 43-bit, not commonly used) and double-extended precision (≥ 79-bit, usually implemented with 80 bits). The basic format for single precision is further divided into sign, exponent, and mantissa part as shown in Fig 3.1.

FIG 3.1: FORMAT FOR DOUBLE-PRECISION MULTIPLIER

3.1 Normalized Numbers [8]

In most cases, the floating-point real numbers are represented in normalized form. A normalized real number consists of a normalized significand that represents a real number between 1 and 2 and an exponent that specifies the number's binary point. The requirement that the leftmost digit of the significand be nonzero is called normalization.

3.2 Real Numbers and non number Encodings

A variety of real numbers and special values can be encoded in floating-point format. These numbers and values are generally divided into the following classes:

1. Signed Zeros

Zero can be represented as a +0 or a -0 depending on the sign bit. Both encodings are equal in value. The sign of a zero result depends on the operation being performed and the rounding mode being used.

2. Normalized and Denormalized Finite Numbers

Non-zero, finite numbers are divided into two classes: normalized and denormalized. The normalized finite numbers comprise all the non-zero finite values that can be encoded in a normalized real number format between zero and infinity (∞). The denormalized number is computed through a technique called gradual underflow.

3. Signed Infinities

The two infinities, +∞ and -∞, represent the maximum positive and negative real numbers, respectively, that can be represented in the floating-point format. Infinity is always represented by a zero significand (fraction and integer bit) and the maximum biased exponent allowed in the specified format

4. Not a Number (NaN)

There are two classes of NaN: quiet NaNs (QNaNs) and signaling NaNs (SNaNs). A QNaN is a NaN with the most significant fraction bit set; a SNaN is a NaN with the most significant fraction bit clear.

5. Indefinite

For each FPU data type, one unique encoding is reserved for representing the special value indefinite.

3.3 Conversion and Rounding

When a number is represented in some other format (such as a string of digits), then it will require a conversion to be used in floating-point format. When the result is obtained from an operation, it may not be possible to represent exactly in the IEEE 754 standard. Therefore, rounding is needed before the result is stored in the memory or registers, and/or sent to the output. In round to nearest even the value is rounded up or down to the nearest infinitely precise result. In round up and down the number will be rounded up towards +∞ and -∞ respectively. Round towards zero modes is not used in general.

3.4 Exceptions

There are four types of exceptions that should be signaled through a one bit status flag when encountered. Some arithmetic operations are invalid, such as a division by zero or square root of a negative number. The result of an invalid operation shall be a NaN.

Inexact exception should be signaled whenever the result of an arithmetic operation is not exact due to the restricted exponent and/or precision range. Two events cause the underflow exception to be signaled, tininess and loss of accuracy. The overflow exception is signaled whenever the result exceeds the maximum value that can be represented due to the restricted exponent range. It is not signaled when one of the operands is infinity, because infinity arithmetic is always exact.

3.5 Multiplication Algorithm

A binary floating-point number is represented by a sign bit, the significand and the exponent. Given two numbers Operand A and Operand B, the flowchart in figure 2 can be used to compute their product, given that e_A, e_B and $frac_A$, $frac_B$ are the exponents and significands of the numbers, respectively. A detailed description of the algorithm follows:

1. The hidden bit (24^{th} bit) is made explicit. If ^{e}a or $^{e}b = 0$, it is made '0', otherwise a '1'.

2. The result of the multiplication is given by the formula:

Sign =$sign_A$ xor $sign_B$, e = $e_A + e_B$,

Frac = $frac_A$ x $frac_B$

The addition of the exponents is a trivial operation as long as we keep in mind that they are biased. This means that in order to get the right result, we have to subtract 127 (bias) from their sum. The sign of the result is just the XOR of the two sign bits. The multiplication of the significands is just an unsigned, integer multiplication.

3. There must be a leading '1' in the significand of any floating-point number (unless it is not denormalized). To make the MSB '1' in the result, the bits are shifted left, and with each shift, the exponent is incremented by 1. This way normalization is done.

3.6 Vedic Multiplier

The multiplier A[n] is of size 'n' words and the multiplicand B[m] is of size 'm' words, where A and B are given by equation 1 and 2**.**

$$A[n] = \sum_{i=0}^{n-1} a_i * X^i \quad (1)$$

$$B[m] = \sum_{i=0}^{m-1} b_i * X^i \quad (2)$$

Product of A and B is given by equation 3.

P [n + m] = A [n] * B [m] (3)

$$\sum_{i=1}^{n} CP[0,0,i] * X^{i-1} +$$

$$\sum_{j=1}^{m-n} CP[0,\ j,n] * X^{n+j-1} +$$

$$\sum_{k=1}^{n-1} CP[k, k+m-n, n-k] * X^{m+k+1}$$

Where

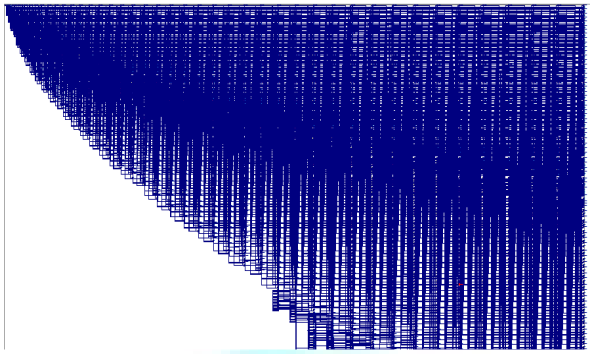
$$CP[n,m,q] = \sum_{i=n}^{n+q-1} a_i * b_j \quad (4)$$

Equation 4 gives the cross-product of two numbers. where j = (m+ n + q - i -1)

4. RESULTS

The code is written in HDL, synthesized and simulated using Virtex 4 (Device : xc4vsx35-10-ff668) and speed grade of -12. Technology schematics is shown in Fig. 4.1.

FIG-4.1: TECHNOLOGY SCHEMATICS



Synthesis results shows 12447 slices are used out of 15360, 22789 numbers of 4 input LUTs are used out of 30720 and number of bonded IOBs are 195 out of 448. This is shown in Fig.4.2.

FIG-4.2: SYNTHESIS RESULTS

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	12447	15360	81%
Number of Slice Flip Flops	144	30720	0%
Number of 4 input LUTs	22789	30720	74%
Number of bonded IOBs	195	448	43%
Number of GCLKs	1	32	3%

Macro Statistics details are given below:

# Adders/Subtractors	: 252
9-bit adder	: 103
12-bit adder	: 2
12-bit subtractor	: 1
16-bit adder	: 1
17-bit adder	: 4
18-bit adder	: 14

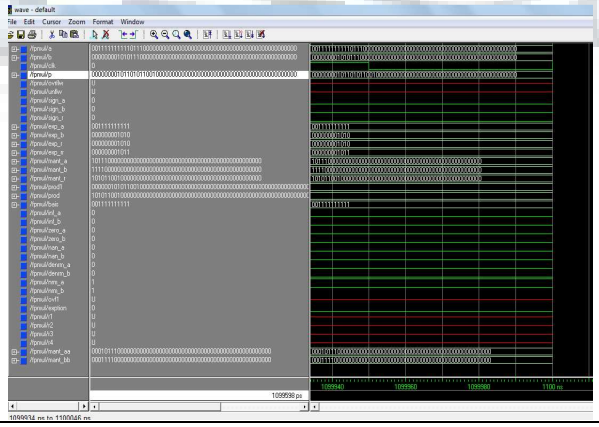
5. CONCLUSION

In this paper, it is shown that double precision floating point multiplier is synthesized and simulated using Configurable devices. The presented implementations give

19-bit adder	: 29
9-bit adder	: 49
# Registers	: 18
1-bit register	: 15
12-bit register	: 1
53-bit register	: 1
64-bit register	: 1
# Comparators	: 8
12-bit comparator greater	: 2
12-bit comparator less	: 2
53-bit comparator equal	: 2
53-bit comparator greater	: 2
# Multiplexers	: 1
109-bit 4-to-1 multiplexer	: 1
# Xors	: 5538
1-bit xor2	: 5538
8 bit adder	: 49

Timing report summary indicates total time taken for process is 203.817 ns out of which 79,879 ns are used for logic and 18.755ns are utilized for routing. Simulation Results are shown in Fig. 4.3.

FIG: 4.3: SIMULATION RESULTS



Since area and speed of the design is always a main concern, finding possible ways of customizing our design in terms of timing delay and slices has been tried and this can also be a future enhancement of the present work. In the end, it can be perceived that such a design can enable substantial savings of resources in the FPGA when used for signal processing applications.

REFERENCES

1. John L. Hennessy and David A. Patterson, "Computer Architecture: A Quantitative Approach", Second Edition, Morgan Kaufmann, 1996.
2. Deschamps, Jean-Pierrie and Sutter, D. Gustavo, "Synthesis of Arithmetic Circuits, FPGA, ASIC and Embedded Systems", John Wiley & sons Inc. Publication (2006).
3. Jagadguru Swami Sri Bharath, Krsna Tirathji, "Vedic Mathematics or Sixteen Simple Sutras from the Vedas", Motilal Banarsidas, Varanasi, India, 1986.
4. Loucas Louca, Todd A. Cook, William H. Johnson, "Implementation of IEEE Single Precision Floating Point Addition and Multiplication on FPGAs", IEEE, Sept. 1996.
5. C.P. Jeannerod, S. Raina and A. Tisserand, " High-Radix Floating-Point Division algorithms for Embedded VLSI Processors", Arenaire Project, 2003.
6. GH. A. Aty, Aziza 1. Hussein, I. S. Ashour and M. Mona,"Highspeed,Area-Efficient FPGA-Based -Floating-point Multiplier",Proceedings ICM 2003, pp-274-277,Dec. 9-11 2003, Cairo, Egypt.
7. Saha, P.Banerjee, A.Dandapat, A.Bhattacharyya, "Vedic Mathematics Based 32-Bit Multiplier Design for High Speed Low Power Processors", International Journal On Smart Sensing And Intelligent Systems, Vol. 4, No. 2, June- 2011,P-268.
8. Dinesh Kumar and Dr. G.C. Lal, "Simulation and Synthesis of 32-Bit Multiplier Using Configurable Devices",International Journal on Advances in Engineering and Technology.Vol 5, Issue2,P-216-222.
9. H. Thapliyal and M. B. Srinivas, "High Speed Efficient N XN Bit Parallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics", Enformatika Trans., vol. 2, pp. 225-228, December 2004.
10. Nabeel Shirazi, A1 Walters, and Peter Athanas."Quantitative Analysis of Floating Point Arithmetic on FPGA Based Custom Computing Machines". In IEEE Symposium on FPGAs for Custom Computing Machines, pages 155-162, April 1995.
11. S.E. Cquillan, J.V. McCanny, and R. Hamill, "New Algorithms and VLSI Architectures for SRT Division and Square Root," Proc. 1I h symp. Computer arithmetic, pp. 80-86, Windsor, Ontario, Canada, June 29-jully 2, 1993.
12. M. E. Louie and M. D. Ercegovac," On Digit -Recurrence Division Implementations for Field Programmable gate Arrays" In Proc. Of the 10th symposium on Computer Arithmetic, PP. 202-209, Canada, June 29 -July 2 ,1993

REQUEST FOR FEEDBACK

Dear Readers

At the very outset, International Journal of Research in Computer Application and Management (IJRCM) acknowledges & appreciates your efforts in showing interest in our present issue under your kind perusal.

I would like to request you tosupply your critical comments and suggestions about the material published in this issue as well as on the journal as a whole, on our E-mail**infoijrcm@gmail.com** for further improvements in the interest of research.

If youhave any queries please feel free to contact us on our E-mail **infoijrcm@gmail.com**.

I am sure that your feedback and deliberations would make future issues better – a result of our joint effort.

Looking forward an appropriate consideration.

With sincere regards

Thanking you profoundly

Academically yours

Sd/-

Co-ordinator

ABOUT THE JOURNAL

In this age of Commerce, Economics, Computer, I.T. & Management and cut throat competition, a group of intellectuals felt the need to have some platform, where young and budding managers and academicians could express their views and discuss the problems among their peers. This journal was conceived with this noble intention in view. This journal has been introduced to give an opportunity for expressing refined and innovative ideas in this field. It is our humble endeavour to provide a springboard to the upcoming specialists and give a chance to know about the latest in the sphere of research and knowledge. We have taken a small step and we hope that with the active co-operation of like-minded scholars, we shall be able to serve the society with our humble efforts.

Our Other Journals